UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/061,474	01/31/2002	Steven Teig	SPLX.P0097	3694

48947 7590 10/30/2006

STATTLER, JOHANSEN, AND ADELI LLP
1875 CENTURY PARK EAST SUITE 1360
LOS ANGELES, CA 90067

EXAMINER	
ORTIZ, BELIX M	

ART UNIT	PAPER NUMBER
2164	

DATE MAILED: 10/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/061,474	TEIG ET AL.
	Examiner	**Art Unit**
	Belix M. Ortiz	2164

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. In response to communications files on 10-October-2006. Therefore, claims 1-25 are presently pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-19 and 24-25 are rejected under 35 U.S.C. 103(a) (Eff. Filing date of application: 1/31/2002) as being unpatentable over Andreev et al. (U.S. pat. 6,587,990)(Eff. Filing date of application: 10/1/2000) in view of Mano et al. (Eff. Filing date: 1984).

As to claim 1, Andreev et al. teaches a data storage structure that stores a plurality of combinational-logic sub-networks (see column 1, lines 36-39 and column 8, lines 2-3), wherein each sub-network performs a set of output functions and comprises a set of circuit elements, at least some of the sub-network comprising a first circuit having a first output outside the sub-network and a second circuit having a second output outside the sub-network, wherein the first circuit receives a direct or indirect input from the second circuit, wherein each sub-network is stored based on a set of indices derived from a set of output functions performed by the sub-

network, the set of indices being used to retrieve the sub-network from the data storage structure (see col. 13, 60-65) within constructing a circuit sheaf (sub-networks) for the combinational circuit with computation of F-sets (output functions) (col. 1, 38-42) and as shown on the Fig. 5 illustrating the a cell 46 (sub-network) within combinational circuit S 40, wherein cell 46 is a group of one or more circuit elements to perform a function such as Q (Boolean logic function is output of sub-network) shown on the truth tables 1A-3A for different sub-circuits (sub-networks) (col. 1, 16-18), (see col. 10, lines 53-64 and col. 6, lines 33-39) where he teach function outputs of sub-network have been stored previously.

Andreev et al. does not teach the specifics regarding the structure of the sub-network.

Mano et al. teaches a sub-network that performs a set of output function, in which he teaches the sub-network comprising a first circuit having a first output outside the sub-network and a second circuit having a second output outside the sub-network, wherein the first circuit receives a direct or indirect input from the second circuit (see figures 3-19 (c) page 91; figures 6-12, page 214; and figures 6-13, page 215).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Andreev et al. by the teaching of Mano, because the sub-network is a group of one or more circuit elements grouped and connected to perform a function.

As to claim 2, Andreev et al. teaches a data storage structure that stores a plurality of combinational-logic sub-networks (see column 1, lines 36-39 and column 8, lines 2-3), wherein each sub-network performs a set of output functions and comprises a set of circuit elements, at least some of the sub-network comprising a first circuit having a first output outside the sub-

network and a second circuit having a second output outside the sub-network, wherein the first circuit receives a direct or indirect input from the second circuit, wherein the data storage structure stores each sub-network based on a parameter derived from a set of output functions of the sub-network, the parameter being used to retrieve the sub-network from the data storage structure (see col. 13, 60-65) within constructing a circuit sheaf (sub-networks) for the combinational circuit with computation of F-sets (output functions) (col. 1, 38-42) and as shown on the Fig. 5 illustrating the a cell 46 (sub-network) within combinational circuit S 40, wherein cell 46 is a group of one or more circuit elements to perform a function such as Q (Boolean logic function is output of sub-network) shown on the truth tables 1A-3A for different sub-circuits (sub-networks) (col. 1, 16-18), (see col. 10, lines 52-57) where he teach function outputs of sub-network have been stored previously in view of the parameter.

Andreev et al. does not teach the specifics regarding the structure of the sub-network.

Mano et al. teaches a sub-network that performs a set of output function, in which he teaches the sub-network comprising a first circuit having a first output outside the sub-network and a second circuit having a second output outside the sub-network, wherein the first circuit receives a direct or indirect input from the second circuit (see figures 3-19 (c) page 91; figures 6-12, page 214; and figures 6-13, page 215).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Andreev et al. by the teaching of Mano, because the sub-network is a group of one or more circuit elements grouped and connected to perform a function.

As to claims 3 and 14, Andreev et al. as modified teaches wherein the parameter for each sub-network is a set of indices for storing the sub-network in the storage structure, wherein the set of indices includes an index for each function performed by the sub-network (see Andreev et al., column 6, 38-42).

As to claims 4 and 15, Andreev et al. as modified teaches wherein the indices are numerical indices (see Andreev et al., column 10, 20-26).

As to claims 5 and 16, Andreev et al. as modified teaches wherein the storage structure is a relational database, and the set of indices are indices into the relational database (see Andreev et al., figure 19; column 11, lines 54-56).

As to claims 6 and 17, Andreev et al. as modified teaches wherein the set of indices for each sub-network includes a primary index and a set of secondary indices (see Andreev et al., figure 19, and column 10, lines 20-26).

As to claims 7 and 18, Andreev et al. as modified teaches wherein the set of secondary indices for a sub-network that only performs one function is empty (see Andreev et al., column 9, lines 64-67).

As to claims 8 and 19, Andreev et al. as modified teaches wherein each sub-network receives a set of inputs, and each sub-network's primary index is the index derived from a pivot

function of the sub-network that depends on all the inputs in the sub-network's set of inputs (see Andreev et al., figures 17 –18 and column 10, lines 7-16).

As to claim 9, Andreev et al. as modified teaches wherein each sub-network's set of indices specify the location where the sub-network is stored in the data storage structure (see Andreev et al., figure 19 and column 11, lines 54-56).

As to claim 10, Andreev et al. as modified teaches wherein the data storage structure stores each sub-network in terms of

(i) a graph that represents the topology of the set of circuit elements of each sub-network, wherein the graph includes a node for each circuit element of the sub-network (see Andreev et al., figure 18 and column 10, lines 15-16)

(ii) a set of local functions that includes a local function for each node of the graph (see Andreev et al., column 11, lines 20-26),

wherein the data storage structure stores, for each sub-network, an identifier that specifies the locations that store the set of local functions and the graph of the sub-network (see Andreev et al., column 8, lines 58-62),

wherein each sub-network's set of indices is associated with the identifier for the sub-network (see Andreev et al., column 11, lines 54-56 and column 8, lines 61-62).

As to claim 11, Andreev et al. as modified teaches wherein each sub-network's identifier includes a graph index and a set of function indices, wherein, for each sub-network, the graph

index identifies the storage location of the graph for the sub-network, and each function index identifies the storage location of a local function of the sub-network (see Andreev et al., figure 19).

As to claim 12, Andreev et al. teaches a sub-network record management system comprising:

a) a data storage structure that stores a plurality of combinational-logic sub-networks (see column 1, lines 36-39 and column 8, lines 2-3), wherein each sub-network performs a set of output functions and comprises a set of circuit elements, at least some of the sub-network comprising a first circuit having a first output outside the sub-network and a second circuit having a second output outside the sub-network, wherein the first circuit receives a direct or indirect input from the second circuit, wherein the data storage structure stores each sub-network based on a parameter derived from a set of output functions of the sub-network, the parameter being used to retrieve the sub-network from the data storage structure (see col. 13, 60-65) within constructing a circuit sheaf (sub-networks) for the combinational circuit with computation of F-sets (output functions) (col. 1, 38-42) and as shown on the Fig. 5 illustrating the a cell 46 (sub-network) within combinational circuit S 40, wherein cell 46 is a group of one or more circuit elements to perform a function such as Q (Boolean logic function is output of sub-network) shown on the truth tables 1A-3A for different sub-circuits (sub-networks) (col. 1, 16-18), (see col. 10, lines 52-57) where he teach function outputs of sub-network have been stored previously in view of the parameter.

b) a data access manager that identifies and retrieves sub-networks from the data storage structure (see column 4, lines 17-30).

Andreev et al. does not teach the specifics regarding the structure of the sub-network.

Mano et al. teaches a sub-network that performs a set of output function, in which he teaches the sub-network comprising a first circuit having a first output outside the sub-network and a second circuit having a second output outside the sub-network, wherein the first circuit receives a direct or indirect input from the second circuit (see figures 3-19 (c) page 91; figures 6-12, page 214; and figures 6-13, page 215).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Andreev et al. by the teaching of Mano, because the sub-network is a group of one or more circuit elements grouped and connected to perform a function.

As to claim 13, Andreev et al. as modified teaches wherein when the data access manager receives a parameter, the manager searches the data storage structure for sub-networks that are stored based on the received parameter, and if the manager finds a sub-network that is stored based on the received parameter, the manager retrieves the sub-network (see Andreev et al., column 10, lines 20-26 and column 11, lines 54-56).

As to claim 24, Andreev et al. as modified teaches wherein at least some sub-networks perform at least tree output functions (see Mano et al., pages 91 and 214).

As to claim 25, Andreev et al. as modified teaches wherein at least some sub-networks perform at least tree output functions (see Mano et al., pages 91 and 214).

4. Claims 20-23 are rejected under 35 U.S.C. 103(a) (Eff. Filing date of application: 1/31/2002) as being unpatentable over Andreev et al. (U.S. pat. 6,587,990)(Eff. Filing date of application: 10/1/2000) in view of Mano et al. (Eff. Filing date: 1984) as applied to claims 1-19 and 24-25 above, and further in view of Pedersen et al. (U.S. 6,134,705) (Eff. Filing date of application: 10/27/1997).

As to claim 20, Andreev et al. as modified still does not teach wherein when the manager receives a set of indices, the manager searches the data storage structure to find a set of indices that match the received set of indices, and if the manager finds a matching set, the manager retrieves the sub-network identified by the matching set.

Pedersen et al. teaches generation of sub-netlists for use in incremental compilation (see abstract) in which he teaches wherein when the manager receives a set of indices, the manager searches the data storage structure to find a set of indices that match the received set of indices, and if the manager finds a matching set, the manager retrieves the sub-network identified by the matching set (see Pedersen et al., column 11, lines 23-26).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Andreev et al. by the teaching of Pedersen, because wherein when the manager receives a set of indices, the manager searches the data storage structure to find a set of indices that match the received set of indices, and if the manager finds a

matching set, the manager retrieves the sub-network identified by the matching set, would enable the record management system to find the information faster.

As to claim 21, Andreev et al. as modified teaches wherein for each particular index pair formed by the received primary index and one of the received secondary indices (see Pedersen et al., figure 7D, characters 762, 764, 766, and 776),

the manager identifies each sub-network stored in the storage structure that is associated with the particular index pair (see Pedersen et al., figure 4A-4B and column 11, lines 62-66),

the manager then determines whether any of the identified sub-networks are associated with all the index pairs (see Pedersen et al., figure 4A-4B and column 11, lines 62-66), and

if so, the manger retrieves any sub-network that is associated with all index pairs (see Pedersen et al., figure 3A).

As to claim 22, Andreev et al. as modified teaches wherein the data storage structure stores each sub-network in terms of

(i) a graph that represents the topology of the set of circuit elements of each sub-network, wherein the graph includes a node for each circuit element of the sub-network (see Andreev et al., figure 18 and column 10, lines 15-16)

(ii) a set of local functions that includes a local function for each node of the graph (see Andreev et al., column 11, lines 20-26),

wherein the data storage structure stores, for each sub-network, an identifier that

specifies the locations that store the set of local functions and the graph of the sub-network (see Andreev et al., column 8, lines 58-62),

wherein each sub-network's set of indices is associated with the identifier for the sub-network (see Andreev et al., column 11, lines 54-56 and column 8, lines 61-62).

As to claim 23, Andreev et al. as modified teaches wherein each sub-network's identifier includes a graph index and a set of function indices, wherein, for each sub-network, the graph index identifies the storage location of the graph for the sub-network, and each function index identifies the storage location of a local function of the sub-network (see Andreev et al., figure 19).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Belix M. Ortiz whose telephone number is 571-272-4081. The examiner can normally be reached on moday-friday 9am-5pm.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

bmo

October 24, 2006

C. Rones

CHARLES RONES
SUPERVISORY PATENT EXAMINER